REMARKS

Claims 16, 22, 27, 30 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshitomi (U.S. Patent Number 6,740,974). Claims 37-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Ogawa, *et al.* (U.S. Publication Number 2003/0012117). In view of the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 16-33, a dual damascene interconnection structure with a metal-insulator-metal capacitor includes a via-level intermetal dielectric and a trench-level intermetal dielectric which are sequentially stacked on a substrate. A dual damascene interconnection is formed in the via-level intermetal dielectric and the trench-level intermetal dielectric. The dual damascene interconnection includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric. A metal-insulator-metal capacitor is formed between the via-level intermetal dielectric and the trench-level intermetal dielectric to include a lower electrode, a dielectric layer and an upper electrode.

Yoshitomi discloses a metal-insulator-metal capacitor 20 formed on a diffusion-preventing film 15, and a third inter-layer film 21 formed on the diffusion-preventing film 15, thus covering the capacitor 20. The capacitor 20 is formed between the diffusion-preventing film 15 and the third inter-layer film 21. No trench is formed to the third inter-layer film 21. A fourth inter-layer film 22 is formed on the third inter-layer film 21 and a fifth interlayer film 23 is formed on the fourth inter-layer film 22. A wiring trench 25c is formed in the fifth inter-layer film 23 and partially through the fourth inter-layer film 22, and a via hole 24c is formed partially through the fourth inter-layer film 22, the third inter-layer film 21 and the diffusion-preventing film 15. Second wiring 27c is formed in the wiring trench 25c and the via hole 24c.

Yoshitomi fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a dual damascene interconnection which includes a line trench extending through the trench-level intermetal dielectric to the via-level intermetal dielectric, as claimed in claims 16-33. The Examiner refers to Yoshitomi's third inter-layer film 21 as the applicant's claimed via-level dielectric and Yoshitomi's fourth inter-layer film 22 as the applicant's claimed trench-level dielectric.

However, in Yoshitomi, wiring trench 25c is formed in the fifth inter-layer film 23 and partially through the fourth inter-layer film 22, not through the fourth inter-layer film 22 to the third inter-layer film 21. Therefore, Yoshitomi does not show the applicant's claimed line trench extending through a trench-level intermetal dielectric to a via-level intermetal dielectric. In Yoshitomi, no trench is formed to the third inter-layer film 21, and therefore the trench does not extend through a trench-level intermetal dielectric to a via-level intermetal dielectric, as claimed by the applicant.

Yoshitomi further fails to teach or suggest a dual damascene interconnection structure that includes a metal-insulator-metal capacitor formed between a via-level intermetal dielectric and a trench-level intermetal dielectric. Instead, in Yoshitomi, the capacitor 20 is formed between a diffusion-preventing film 15 and a third inter-layer film 21.

Yoshitomi fails to teach or suggest elements of the invention set forth in claims 16-33. Specifically, Yoshitomi fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor that includes a dual damascene interconnection which includes a line trench extending through a trench-level intermetal dielectric to a via-level intermetal dielectric and a metal-insulator-metal capacitor formed between the via-level intermetal dielectric and the trench-level intermetal dielectric, as claimed in claims 16-33. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claims 16, 22, 27, 30 and 31 under 35 U.S.C. 102(e) as being anticipated by Yoshitomi, is respectfully requested.

With regard to the rejection of claims 37-39 as being anticipated by Ogawa, *et al.*, claims 38 and 39 are cancelled. In the present invention as claimed in claim 37, a dual damascene interconnection structure with a metal-insulator-metal capacitor includes a via-level intermetal dielectric and a trench-level intermetal dielectric which are sequentially stacked on a substrate. A dual damascene interconnection is formed in the via-level intermetal dielectric and the trench-level intermetal dielectric. A metal-insulator-metal capacitor is formed between the via-level intermetal dielectric and the trench-level intermetal dielectric to include a lower electrode, a dielectric layer and an upper electrode. The lower electrode is formed on the via-level intermetal dielectric. A first lower metal interconnection is formed between the substrate and the via-level

intermetal dielectric. The lower electrode extends through the via-level intermetal dielectric and is directly connected to the first lower metal interconnection.

Claim 37 is amended to clarify that the lower electrode is formed on the via-level intermetal dielectric and extends through the via-level intermetal dielectric to be directly connected to the first lower metal interconnection. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

Ogawa, *et al.* discloses that a dummy lower electrode 33b is formed on a dummy barrier metal 32b. The dummy barrier metal 32b contacts a dummy cell plug 30b, and the dummy cell plug contacts a local interconnect 21b. The lower electrode 33b is connected to the local interconnect 21b through the dummy barrier metal 32b and the dummy cell plug 30b.

Ogawa, *et al.* fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor which includes a lower electrode which is formed on a via-level intermetal dielectric and extends through the via-level intermetal dielectric and is directly connected to a first lower metal interconnection, as claimed in claim 37. Instead, in Ogawa, *et al.*, the lower electrode 33b is connected to the local interconnect 21b through the dummy barrier metal 32b and the dummy cell plug 30b. Therefore, the lower electrode 33b does not extend through a via-level intermetal dielectric and is not directly connected to the local interconnect 21b.

Ogawa, *et al.* fails to teach or suggest elements of the invention set forth in claim 37. Specifically, Ogawa, *et al.* fails to teach or suggest a dual damascene interconnection structure with a metal-insulator-metal capacitor which includes a lower electrode which extends is formed on a via-level intermetal dielectric and is directly connected to a first lower metal interconnection, as claimed in claim 37. Therefore, it is believed that the claim is allowable over the cited reference, and reconsideration of the rejections of claim 37 under 35 U.S.C. 102(e) as being anticipated by Ogawa, *et al.*, is respectfully requested.

In view of foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to

issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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